What is claimed:

1. A semiconductor device comprising:

a pad which is formed on an insulating layer and has an electric connection region to connect with external components; and

a protective insulating layer which is formed on the insulating layer and the pad and has an aperture for exposing the electric connection region,

wherein at least part of a side surface of the protective insulating layer surrounding the electric connection region is a tapered surface with an acute angle to a top surface of the pad; and

wherein the protective insulating layer includes at least first and second insulating layers, each of which has a side surface exposed to the aperture.

2. The semiconductor device of claim 1,

wherein an etching rate of a material forming the first insulating layer is different from an etching rate of a material forming the second insulating layer.

3. The semiconductor device of claim 1,

wherein the first insulating layer is formed on the insulating layer; and

wherein the second insulating layer is formed on the first insulating layer.

4. The semiconductor device of claim 1,

wherein the second insulating layer is larger than the first insulating layer in thickness.

5. The semiconductor device of claim 4,

wherein the first insulating layer has a thickness of 400 nm to 600 nm; and

wherein the second insulating layer has a thickness of 600 nm to 1400 nm.

6. The semiconductor device of claim 1,
wherein at least the side surface of the second insulating layer exposed to the aperture is a tapered surface with an acute angle to the top surface of the pad.

7. The semiconductor device of claim 1,
wherein a tapered angle between the side surface of the second insulating layer exposed to the aperture and the top surface of the pad is smaller than a tapered angle between a side surface of the first insulating layer exposed to the aperture and the top surface of the pad.

8. The semiconductor device of claim 1,
wherein a tapered angle between the side surface of a portion of the second insulating layer exposed to the aperture and the top surface of the pad is in the range of 30° to 60°.

9. The semiconductor device of claim 1,
wherein an angle between the side surface of a portion of the first insulating layer exposed to the aperture and the top surface of the pad is in the range of 60° to 90°.

10. The semiconductor device of claim 1,
wherein the distance between an upper end of the side surface of the first insulating layer exposed to the aperture and a lower end of the side surface of the second insulating layer exposed to the aperture is in the range of 0 μm to 3 μm.

11. The semiconductor device of claim 10,
wherein the distance is in the range of 0 μm to 1 μm.

12. The semiconductor device of claim 1,
wherein the aperture in the second insulating layer is larger than the aperture in the first insulating layer.

13. The semiconductor device of claim 1,
wherein a bump electrode is formed on the electric connection region in the pad through a barrier layer.

14. The semiconductor device of claim 1,
wherein the first and second insulating layer are patterned by means of the same mask layer.

15. The semiconductor device of claim 1,
wherein the first insulating layer is formed of a silicon oxide layer.

16. The semiconductor device of claim 1,
wherein the second insulating layer is formed of a silicon nitride layer.

17. A semiconductor device comprising:
a pad which is formed on an insulating layer and includes an electric connection region with external components; and
a protective insulating layer which is formed on the insulating layer and the pad and includes an aperture over at least part of the electric connection region,
wherein a side surface of the protective insulating layer surrounding the electric connection region is a tapered surface with an acute angle to a top surface of the pad.

18. The semiconductor device of claim 17,
wherein the protective insulating layer has a thickness of 1000 nm to 2000 nm.

19. The semiconductor device of claim 17,
wherein a tapered angle between the side surface of the second insulating layer surrounding the electric connection region and the top surface of the pad is in the range of 10° to 80°.

20. The semiconductor device of claim 17,
wherein a bump electrode is provided on the electric connection region of the pad through a barrier layer.

21. The semiconductor device of claim 17,
wherein the protective insulating layer is formed of one of a silicon oxide layer and a silicon nitride layer.

22. A method of fabricating a semiconductor device comprising:
forming a pad with a predetermined pattern on an insulating layer;
forming a protective insulating layer on the insulating layer and over the pad by sequentially forming at least first and second insulating layers;
forming a mask layer on the protective insulating layer, the mask layer having an aperture in a region corresponding to an electric connection region of the pad; and
selectively etching the first and second insulating layers by using the mask layer as a mask to expose the electric connection region.

23. The method of fabricating a semiconductor device of claim 22,
wherein the second insulating layer is patterned by isotropic etching.

24. The method of fabricating a semiconductor device of claim 22,
wherein the first insulating layer is patterned by anisotropic etching.

25. The method of fabricating a semiconductor device of claim 22, wherein the first and second insulating layers are continuously patterned.

26. The method of fabricating a semiconductor device of claim 22, wherein an etching rate of a material forming the first insulating layer is different from an etching rate of a material forming the second insulating layer.

27. The method of fabricating a semiconductor device of claim 22, wherein the second insulating layer is larger than the first insulating layer in thickness.

28. The method of fabricating a semiconductor device of claim 27, wherein the first insulating layer has a thickness of 400 nm to 600 nm; and wherein the second insulating layer has a thickness of 600 nm to 1400 nm.

29. The method of fabricating a semiconductor device of claim 22, wherein at least a side surface of the second insulating layer surrounding the electric connection region has a tapered surface with an acute angle to the top surface of the pad.

30. The method of fabricating a semiconductor device of claim 22, wherein a tapered angle between the side surface of the second insulating layer surrounding the electric connection region and the top surface of the pad is smaller than a tapered angle between the side surface of the first insulating layer surrounding the electric connection region and the top surface of the pad.

31. The method of fabricating a semiconductor device of claim 22,

wherein a tapered angle between the side surface of a portion of the second insulating layer surrounding the electric connection region and the top surface of the pad is in the range of 30° to 60°.

32. The method of fabricating a semiconductor device of claim 22,

wherein an angle between the side surface of a portion of the first insulating layer surrounding the electric connection region and the top surface of the pad is in the range of 60° to 90°.

33. The method of fabricating a semiconductor device of claim 22,

wherein the distance between an upper end of the side surface of the first insulating layer surrounding the electric connection region and a lower end of the side surface of the second insulating layer surrounding the electric connection region is in the range of 0 μm to 3 μm.

34. The method of fabricating a semiconductor device of claim 33,

wherein the distance is in the range of 0 μm to 1 μm.

35. The method of fabricating a semiconductor device of claim 22,

wherein the aperture in the second insulating layer is larger than the aperture in the first insulating layer.

36. The method of fabricating a semiconductor device of claim 22,

wherein a bump electrode is formed on the electric connection region in the pad through a barrier layer.

37. The method of fabricating a semiconductor device of claim 22,

wherein the first insulating layer is a silicon oxide layer.

38. The method of fabricating a semiconductor device of claim 22, wherein the second insulating layer is a nitride oxide layer.

39. A method of fabricating a semiconductor device comprising:
forming a pad with a predetermined pattern on an insulating layer;
forming a protective insulating layer on the insulating layer over the pad;
forming a mask layer on the protective insulating layer, the mask layer having an aperture in a region corresponding to an electric connection region of the pad; and
patterning the protective insulating layer by isotropic etching with the mask layer as a mask to expose the electric connection region.

40. The method of fabricating a semiconductor device of claim 39, wherein the protective insulating layer has a thickness of 1000 nm to 2000 nm.

41. The method of fabricating a semiconductor device of claim 39, wherein a tapered angle between a side surface of the insulating layer surrounding the electric connection region and the top surface of the pad is in the range of 10° to 80°.

42. The method of fabricating a semiconductor device of claim 39, wherein a bump electrode is provided on the electric connection region of the pad through a barrier layer.

43. The method of fabricating a semiconductor device of claim 39, wherein the protective insulating layer is formed from a material including one of a silicon oxide layer and a silicon nitride layer.

44. A bonding pad structure comprising:

a bonding pad formed over a portion of a substrate;

an insulating region formed over a portion of said bonding pad, wherein the bonding pad includes an area surrounded by and uncovered by the insulating region;

the insulating region including a side surface surrounding the uncovered area of the bonding pad, wherein at least part of the side surface is tapered and has an acute angle to a top surface of the bonding pad.

45. The bonding pad structure of claim 44, wherein the insulating region comprises an upper layer and a lower layer, and the side surface includes an upper layer side surface having an acute angle to a top surface of the bonding pad and a lower layer side surface having an acute angle to a top surface of the bonding pad.

46. The bonding pad structure of claim 45, wherein the upper layer side surface has an angle of 30° to 60° to a surface parallel to a top surface of the bonding pad and the lower side surface has an angle of 60° to 90° to a top surface of the bonding pad.

47. The bonding pad of structure of claim 44, wherein the at least part of the side surface has an angle of 10° to 80° to an upper surface of said bonding pad.